

TTO - IPM Cell



Industrial Consultancy & Sponsored Research (IC&SR)

System and method for automatic parallel code generation for graph algorithms for multiple target architectures **IITM Technology Available for Licensing**

PROBLEM STATEMENT

- Generally, parallelization of graph algorithms unavoidable with the growth unstructured & semi-structured data, & graph algorithms have difficult to parallelize the inherent irregularity computation, memory access communication.
- Further, existing prior framework exploiting the parallelism on different hardware is difficult for different in application domain.
- However, the existing framework unable to address the issues. Therefore, there is need for a system & method for Graph Domain Specific Solution (DSL) to address issues.

TECHNOLOGY CATEGORY/ MARKET

Technology: Graph Domain Specific

Language (DSL) Compiler; Industry: DSL Compiler;

Applications: Hardware & Software for Graph DSL Compiler, System software;

TECHNOLOGY

- The present invention describes a system & method for automatic parallel code generation for graph algorithms for multiple target architectures.
- A graph domain specific language (DSL) named StarPlat framework enables a user to provide an algorithm specification of graph problems (high level graph specific constructs) & generates parallel code for multiple backends from same algorithm specification.
- Said System comprises a user device, a graph algorithm unit, an intermediate representation unit, a code generator unit, a performance analysis unit and a compiler, shown in figure 1.

IMAGES

Graph	Acronym	Num. Vertices	Num. Edges	Diameter	Avg. Degree	Max. Degree
		(million)	(million)			
twitter-2010	TW	21.2	265.0		12	302779
soc-sinaweibo	SW	58.6	261.0		4	4000
orkut	OK	3.0	234.3	9	76.2813	33,313
wikipedia-ru	WK	3.3	93.3	10	55.4067	283,929
livejournal	LJ	4.8	69.0	16	28.257	22,887
soc-pokec	PK	1.6	30.6	11	37.5092	20,518
usaroad	US	24.0	28.9		2	9
germany-osm	GR	11.5	12.4		2	13
rmat876	RM	16.7	87.6		5	128332
uniform-random	UR	10.0	80.0		8	27

Table1: Illustrates as Input Graph for analysis;

KEY FEATURES / VALUE PROPOSITION

- * Technical Perspective: Current method generates the codes for backends simultaneously with efficient parallel processing approach for graph algorithms multiple for architecture (OpenMP, MPI & CUDA).
- ❖ Industrial Perspective: Both static and dynamic graph algorithm can be taken as input & generates code (library or framework based).
- Applicable to High performance computing & parallel computing, compilers.

INTELLECTUAL PROPERTY

IITM IDF Ref. 2422; Patent No: 432922

TRL (TECHNOLOGY READINESS LEVEL)

TRL- 3, Proof of Concept ready & validated

RESEARCH LAB

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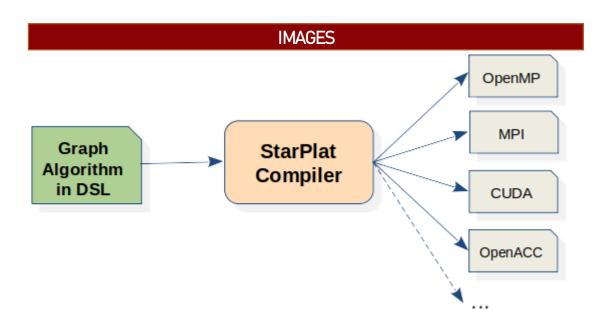


Fig. 1: Illustrates a detailed block diagram of a compiler for automatic parallel code generation of graph algorithm for multiple target architectures.

Experimental Result

Sr. No.	Algorithm		Lines o	of code	Lines of code	Reduction	
		OpenMP	MPI	CUDA	Total	StarPlat	Ratio
1	вс	99	284	222	605	33	18.3
2	PR	42	157	139	338	31	10.9
3	SSSP	54	124	140	318	20	15.9
4	TC	31	60	106	197	18	10.9

Table 2: Illustrates different algorithms analyzed by using proposed system and as an output obtained reduction of lines of code within the same time frame as that of conventional system.

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