A Delta Sigma Modulator with Noise Attenuating Feedback Filters

IITM Technology Available for Licensing

Problem Statement

- Traditional delta-sigma modulators suffer from **quantization noise folding** due to non-idealities in chopping modulation, **degrading signal-to-noise ratio**, at high frequencies.
- **Quantization noise** at 2fchp can fold into the signal band during ADC sampling, elevating the noise floor and **negatively affecting** the **modulator's SNR** and overall performance.
- **Common mode shifts** in differential integrators pose challenges, **leading to changes in** the **difference between outputs** and affecting **accurate signal processing.**
- Hence, there is a need of a new technology to addresses all the above mentioned issues.

Technology Category / Market

Categories: Electronics & Circuits

Industry: ΔΣ Modulation, DAC Bit Width & Loop Configuration, Amplifier, Electronic System & Design Manufacturing (ESDM), High-precision Analog-to-Digital Converters (ADCs)

Applications: IT, Telecom, IoT, Consumer Electronics, Data Converters, Audio Processing, Sensor Interfaces, Automation

Market: The Global Delta-sigma Modulator Market size is expected to grow from **USD 1.57 billion in 2022 to USD 3.24 billion by 2033**, at a **CAGR of 7.5% from 2023 to 2033**.

Technology

The technology disclosed is a **Delta-Sigma Modulator with Noise Attenuating Feedback Filters,** designed to achieve high-performance analog-to-digital conversion with a focus on enhancing the **Signal-to-Noise Ratio (SNR)** & **Signal-to-Noise & Distortion Ratio (SNDR).**

FIG 1A

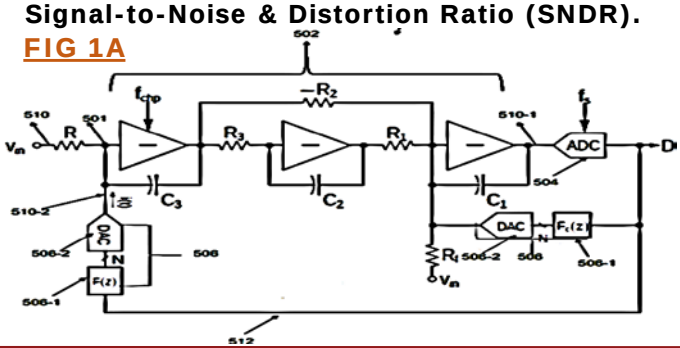
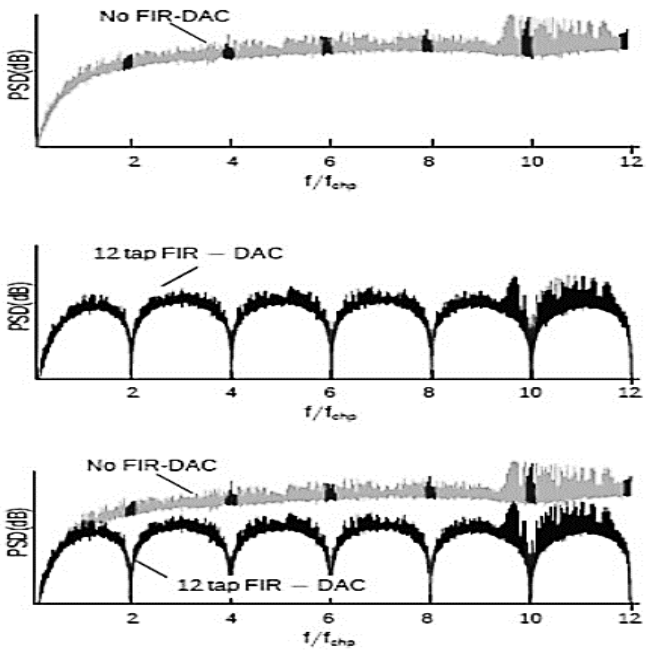


FIG 1A shows a continuous time ΔΣ modulator with a feedback FIR DAC; **FIG 1B** is a graph showing Power Spectral density **PSD** for **FIG 1A.**

FIG 1B



Key Features / Value Proposition

- Emphasize **real-world applications** for precision.
- Specify the benefits of **superior SNR/SNDR**.
- Shows applications where **low power is critical**.
- Explain how modulator get **280 µW efficiency**.
- **Versatile** & Achieves **<10 Hz 1/f noise corner**.
- Modulator is made specifically to **meet the industrial need**. It explains the contribution of chopping frequency & FIR DAC in **optimization**.
- **Cost-efficient** in comparison to alternatives. Key design elements contributing to **economy**.
- Modulator addresses **environment challenges**.
- Provides a practical example of **improved performance**. Shows the impact of **chopping frequency on power consumption.**
- Explains the **contribution of spectral nulls in noise reduction.**
- Offer studies showing **flexibility benefits**, Helps in **strengthening design flexibility effectively**.

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Technology Disclosure

The disclosed patent involves technologies related to delta sigma modulation, specifically focusing on a M-bit delta sigma modulator with noise attenuating feedback filters. The key technologies disclosed include:

Delta Sigma Modulation (ΔΣM):	The core technology revolves around delta sigma modulation, a method for high-resolution analog-to-digital conversion.
Integrator Design:	Design & implementation of integrators, which are crucial components in delta sigma modulators. Integrators generate an integrated signal undergoes further processing.
Loop Filter Configuration:	The loop filter, comprising a cascade of integrators, is an essential part of the delta sigma modulator. The configuration of the loop filter significantly impacts the overall performance of the modulator.
Analog-to-Digital Converter (ADC):	The M-bit ADC is employed to convert the filtered analog signal to a digital signal. It may cover aspects of ADC design and its integration into the modulator.
Feedback Filters:	It introduces noise attenuating feedback filters, specifically FIR filters, in feedback path. These filters play a crucial role in shaping the quantization noise spectrum.
Digital-to-Analog Converter (DAC):	The Q-bit DAC is utilized to convert the filtered digital signal into a negative feedback analog signal. The characteristics of the DAC are likely to be relevant.
Chopping Technique:	Uses chopping at a specific frequency (fchp), contributing to the modulation process.
Spectral Nulls:	The technology involves the introduction of spectral nulls at multiples of 2*(fs/N), where N is greater than 2, to enhance the signal-to-noise characteristics.
FIR Filter Technology:	The FIR filter, with a specific number of taps (L-taps), is employed in the feedback path. Design and characteristics of this filter are disclosed.
Technology Integration:	The patent may cover how these technologies are integrated into a cohesive system to achieve the desired noise reduction and signal fidelity.

TRL (Technology Readiness Level)

TRL - 4, Experimentally validated in lab.

Research Lab

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Intellectual Property

IITM IDF Number: **1317** | Patent Grant Number: **390642** | PCT Number: **PCT/IN2016/050291**

Method for Generating an M-bit Digital Signal

1. **Provide an Analog Input Signal**
2. **Generate an Integrated Signal in an Input Path**
3. **Filter Integrated Signal To Generate A Filtered Analog Signal**
4. **Convert The Filtered Analog Signal To A M-bit Digital Signal**
5. **Generate A Filtered Digital Signal**
6. **Convert The Filtered Digital Signal To A Negative Feedback Analog Signal**

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