CPLD BASED ACTIVE GATE DRIVER FOR HARD SWITCHED AND SOFT SWITCHED SIC MOSFET

IITM Technology Available for Licensing

Problem Statement

- SiC MOSFETs exhibit faster switching speeds than Si IGBTs, leading to excessive overshoot and oscillation in device voltage and current during transients due to L-C network effects.
- There is a need to develop an active gate driver (AGD) to dynamically manage gate capacitance charging and discharging based on real-time device feedback, aiming to mitigate overshoot and oscillation effects during switching.
- Design an AGD system capable of achieving quasi-zero voltage switching (QZV) and quasi-zero current switching (QZC) under various load conditions, thereby minimizing switching losses and addressing EMI issues associated with SiC MOSFET operation.

Intellectual Property

- IITM IDF Ref. **1328**
- **IN 493424 - Patent Granted**

Technology Category/ Market

Power Electronics and Semiconductor Devices
Applications- Renewable Energy Systems, Electric Vehicles (EVs)
Industry - Power Electronics & Automotive

Market - Silicon Carbide Power Semiconductor Market size is estimated at USD 2 billion in 2024, and is expected to reach USD 6.7 billion by 2029, growing at a **CAGR of 25.%** during the 2024-2029.

TRL (Technology Readiness Level)

TRL - 4: Technology validated in lab scale.

Research Lab

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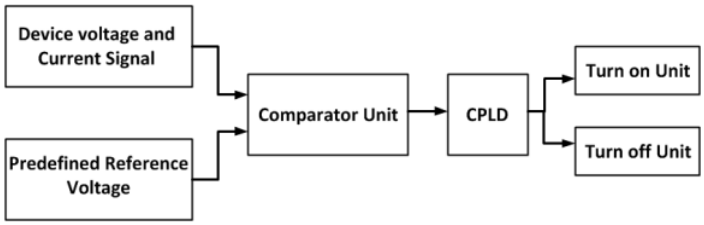

FIG. 1. Block diagram representation of control signal sensing and comparator unit.

Technology

1.Product Description:

- An active gate driver (AGD) is proposed, consisting of turn-on and turn-off mechanisms along with a complex programmable logic device (CPLD).
- The CPLD analyzes input signals from a comparator unit to generate a control signal voltage, facilitating selective switching of one or more transistors' gate terminals.

2. Methodology:

- The AGD dynamically adjusts gate resistance during switching transients, enabling precise control over turn-on and turn-off processes.
- This involves configuring the CPLD to interpret signals from the comparator unit and outputting appropriate control voltages to manage transistor gating effectively.

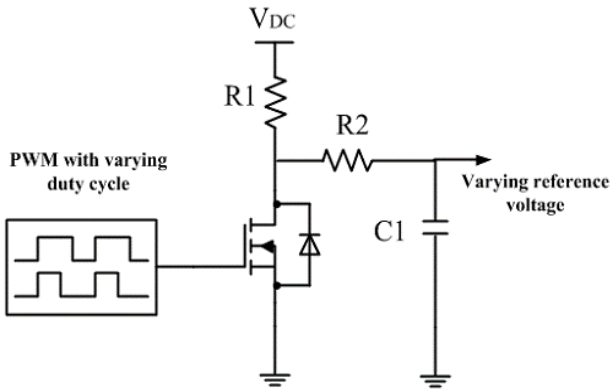

FIG. 2. Shows a mechanism to generate variable reference voltage.

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Images

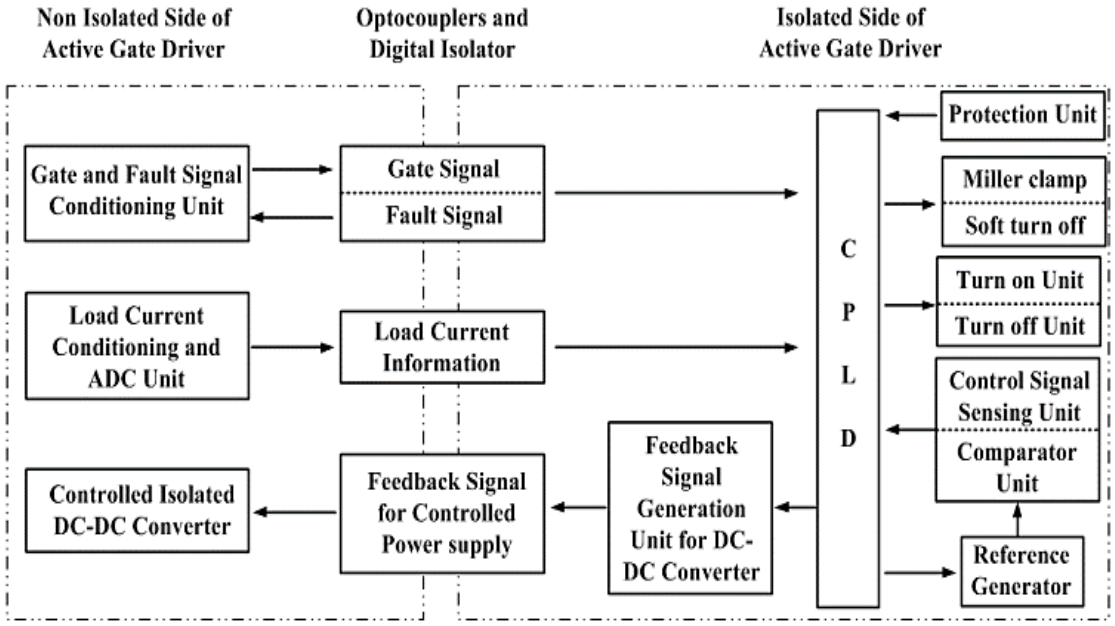

FIG. 3. Block diagram

Key Features / Value Proposition

1. Enhanced Efficiency:	Reduction of voltage and current overshoots leads to decreased switching losses, thereby improving converter efficiency.
2. Oscillation Mitigation	Persistent oscillations in voltage and current are arrested through precise control over parasitic inductance and device capacitance interactions.
3. EMI Reduction:	Control over di/dt and dv/dt, alongside improved common mode noise reduction, enhances EMI performance in hard-switched converters.
4.Optimized Switching:	Complete Quasi-Zero Voltage (QZV) and Quasi-Zero Current (QZC) achievement with controlled gate current injection minimizes switching losses.
5. Advanced Protection:	Reduced blanking time for shoot-through protection ensures continuous device protection during switching intervals.
6. Fault Tolerance:	Soft turn-off feature and gate voltage limitation safeguard device integrity under fault conditions, enhancing reliability across various load scenarios.

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