# CLOSED LOOP ACTIVE GATE DRIVER UNIT USING HIGH BANDWIDTH CONTROLLED CURRENT SOURCE WITH DYNAMIC GATE VOLTAGE CLAMPING

## IITM Technology Available for Licensing

### Problem Statement

- The introduction of SiC-MOSFETs demands a suitable gate driver to manage their fast switching times and prevent voltage and current spikes, which can stress the MOSFET and lead to EMI issues.
- Conventional gate drivers often rely on increasing gate resistance to mitigate issues, but this compromises the benefits of SiC-MOSFETs by increasing switching times and losses
- There's a need for a noise-immune, high-bandwidth analog-based gate driver that can address the specific challenges posed by SiC-MOSFETs, optimizing switching losses, stress on the MOSFET, and EMI/EMC performance.

### Intellectual Property

- IITM IDF Ref. **1488**
- **IN 499369 - Patent Granted**

### Technology Category/ Market

**Category- Power Electronics and Semiconductor Devices.**
**Applications**- Renewable Energy Systems, Electric Vehicles (EVs)
**Industry -** Power Electronics & Automotive

**Market -** Silicon Carbide Power Semiconductor Market size is estimated at USD 2 billion in 2024, and is expected to reach USD 6.7 billion by 2029, growing at a **CAGR of 25.%** during the 2024-2029.

### TRL (Technology Readiness Level)

**TRL - 4: Technology validated in lab scale.**

### Research Lab

**Prof. Kamalesh Hatua,**
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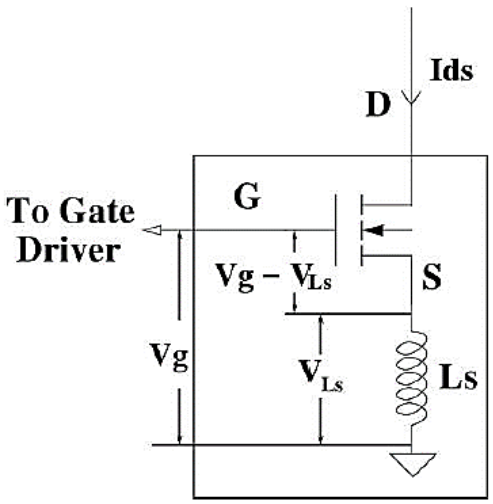


**FIG. 1 Schematic represents inherent di/dt feedback due to common source inductance Ls.**

### Technology

**1. Gate Driver Design**:
The gate driver for SiC-MOSFETs includes components for generating reference voltages based on gate pulses, load current, and drain current. It also incorporates voltage addition, voltage-to-current conversion, RC differentiation, and current amplification stages.

**2. Voltage Clamping Mechanism**:
To regulate gate voltage, the gate driver employs positive and negative voltage clamping circuits, with one circuit set at recommended levels and another set higher to offset common source inductance effects.

**3. Operational Method**:
The method involves generating reference voltages, combining them with feedback signals, converting them into currents, generating a second current through differentiation, and amplifying both currents to supply controlled gate current to the SiC-MOSFET.

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## Key Features / Value Proposition

### 1. SiC-MOSFET Integration

- Addressing the burgeoning demand for gate drivers tailored to the high-speed switching capabilities of Silicon Carbide MOSFETs.

### 2. Enhanced Efficiency:

- Offering precise control over gate currents to minimize switching losses and optimize performance in voltage source converters.

### 3. EMI Mitigation:

- Providing solutions to combat electromagnetic interference (EMI) issues associated with fast-switching SiC-MOSFETs, ensuring compliance with regulatory standards.

### 4. Parallelization Facilitation:

- Enabling easy parallelization of SiC-MOSFETs by leveraging their positive temperature coefficient of ON state drop, enhancing scalability in power electronics applications.

### 5. Analog Precision, Digital Robustness:

- Offering the robustness of analog control with precise feedback mechanisms, ensuring optimal SiC-MOSFET operation while mitigating noise.

### 6. Value-added Innovation:

- Delivering a noise-immune, high-bandwidth analog-based gate driver, catering to the evolving needs of the power electronics industry with a focus on efficiency and reliability.

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