

BI-LAYER RESIST APPROACH OF PHOTOLITHOGRAPHIC PATTERNING OVER PMMA BASED POLYMER DIELECTRICS

IITM Technology Available for Licensing

Problem Statement

- Conventional photoresist processing causes severe degradation of the organic polymers resulting in poor device performance.
- Polymer gate dielectrics/Semiconductors have poor organic solvent resistance while being difficult to process using photolithography.
- Limited progress in the development of photolithography over pristine PMMA or PMMA based polymer dielectrics despite outstanding properties.
- There is a need for developing a method of photolithographic patterning which facilitates the photolithography of PMMA based polymer dielectrics without using high-temperature processing and chemical modification which result in high fabrication cost.

Intellectual Property

- IITM IDF Ref. 1560
- IN 384333 - Patent Granted
- PCT/IN2018/050436

TRL (Technology Readiness Level)

TRL - 4: Technology validated in lab scale.

Technology Category/ Market

Category-Electronics and Circuits

Industry Classification:

- NIC (2008)- 26101- Manufacture of electronic capacitors, resistors, chokes, coils, transformers (electronic) and similar components
- NAICS (2022)- 333242- Thin layer deposition equipment, semiconductor, manufacturing

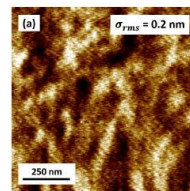
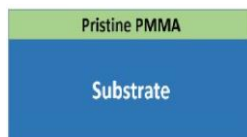
Applications- Semiconductors- Organic Thin Film Transistors (OTFT) for flexible electronics.

Market Drivers-

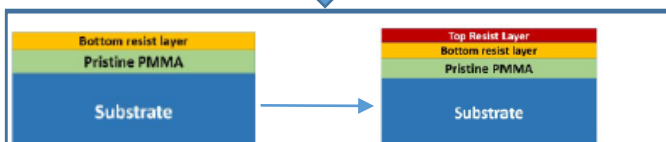
- Increasing demand for flexible displays and electronics- USD 14-15 Billion in 2023; expected CAGR of 33% for 2023-2031

Research Lab

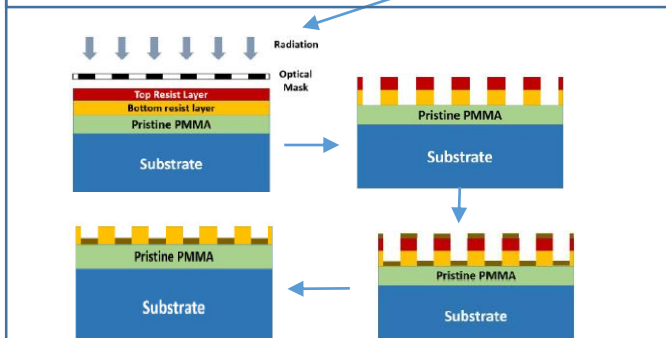
Prof. Soumya Dutta,
Dept. of Electrical Engineering, IITM



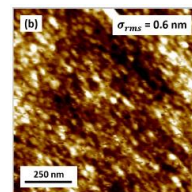
Pristine PMMA layer before processing with AFM image



Bilayer resist formation



UV/Deep exposure through mask, metal deposition and lift off



Pristine PMMA layer after processing the layer through lithographic patterning process of the present invention with AFM image



Fabricated PMMA based Metal-Insulator-Metal (MIM) devices

CONTACT US

Dr. Dara Ajay, Head TTO
Technology Transfer Office,
IPM Cell- IC&SR, IIT Madras

IITM TTO Website:
<https://ipm.icsr.in/ipm/>

Email: smipm-icsr@icsrpiis.iitm.ac.in
sm-marketing@imail.iitm.ac.in

Phone: +91-44-2257 9756/ 9719



BI-LAYER RESIST APPROACH OF PHOTOLITHOGRAPHIC PATTERNING OVER PMMA BASED POLYMER DIELECTRICS

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Technology

- 1 UV/Deep-UV lithography over pristine Poly(methyl methacrylate) (PMMA) or PMMA based hybrid/blended and multilayered polymer dielectric systems using bilayer photoresist stack
- 2 Isopropyl alcohol is used as photoresist stripper for easy stripping of the top resist layer during metal lift-off without dissolving or damaging the PMMA.
- 3 Electrical and dielectric properties of the pristine PMMA layer processed using the invented method was compared to a layer created using shadow mask process fabricated metal-insulator-metal (MIM) device
- 4 Formation of bi-layer resist with MicroChem's PMGI as a bottom resist layer coated directly over pristine PMMA dielectric layer followed by the formation of the top resist layer (typical g-line, i-line, broadband, deep UV, and 193nm resist) by spin coating method. Exposed bi-layer resist stack developed using Shipley's MF319.

Key Features / Value Proposition

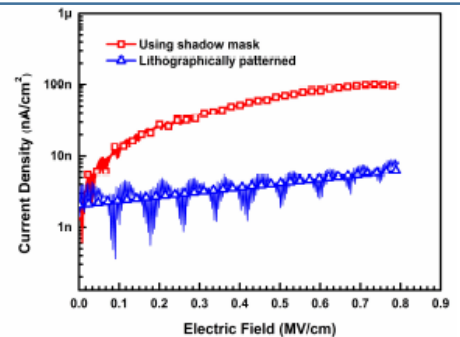
The method **does not involve any complicated process** such as chemical modification or etching of PMMA thus avoiding surface damage.

The **leakage current density in the fabricated device is reduced** almost by two orders of magnitude compared to the device fabricated using a shadow mask.

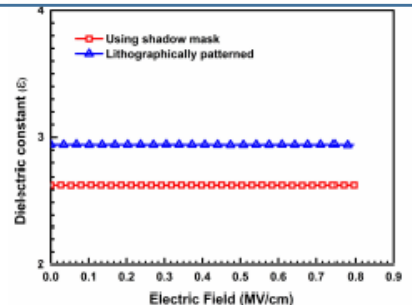
Suitable for bottom gate bottom contact (BGBC), bottom gate top contact (BGTC) and top gate top contact (TGTC) device configuration. These configurations are difficult in case of traditional etching due to surface damage

PMMA dielectric processed by this method shows **good electrical insulating properties. This is better than popular PVP based dielectrics that suffers from affinity to H₂O and severe hysteresis**

The method is **more cost efficient because of the low-temperature processing steps and use of conventional photoresists/developers to perform photolithography**



Leakage current density for two device sets fabricated using a shadow mask and lithographic patterning process of the invention



Dielectric constant as a function of applied electric field for two device sets fabricated using a shadow mask and lithographic patterning process of the present invention

CONTACT US

Dr. Dara Ajay, Head TTO
Technology Transfer Office,
IPM Cell- IC&SR, IIT Madras

IITM TTO Website:
<https://ipm.icsr.in/ipm/>

Email: smipm-icsr@icsrpiis.iitm.ac.in
sm-marketing@imail.iitm.ac.in

Phone: +91-44-2257 9756/ 9719