PHASE ERROR MEASUREMENT CIRCUIT WITH REFERENCELESS GAIN AND OFFSET CALIBRATION

IITM Technology Available for Licensing

Problem Statement

- Static phase errors in **high-frequency periodic signals cause performance degradation** in signal processing ICs, impacting image rejection, error vector magnitude, adjacent channel power ratio, and bit error rate.
- Current **solutions lack accurate phase error** measurement without a reference signal and effective compensation methods to eliminate phase errors.

Technology Category/ Market

Category – Electrical Engineering, Circuit Diagnostics
Applications –Electronic System & Design Manufacturing, ICT, Automotive
Industry – IT Hardware, Test Equipment, Wireless
Market - Electronic Design Automation Market was valued at USD 12.9 billion in 2022 and is estimated to register **a CAGR of over 10%** between 2023 and 2032.

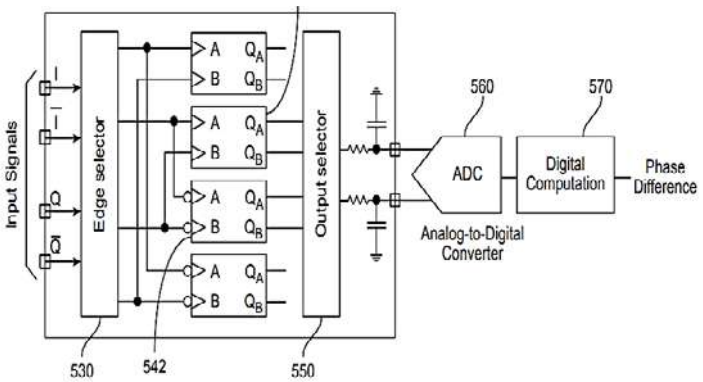

FIG. 1: illustrates an integrated circuit chip incorporating the error compensating circuit architecture.

Research Lab

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Technology

Gain and Offset-Calibrated 3-State Phase Detector:
Utilizes calibrated gain and offset parameters to accurately measure phase differences between signals, crucial for high-frequency signal processing ICs.

Error-Compensating Circuit Architecture:
Utilizes a weighted sum of input voltages and one-port networks to achieve tunable delays.

Integrated Circuit Chip for Phase Error Measurement:
Develops specialized chips capable of directly measuring phase errors without requiring a reference signal, enabling precise phase correction in various applications.

System-on-Chip Implementation:
Integrates phase error measurement functionality into system-on-chip architectures, streamlining the design process and enhancing the efficiency of signal processing systems.

Application in SSB Up/Down Converters and Phase Modulators:
Addresses specific needs in communication devices by detecting and correcting phase errors in local oscillator signals and output signals, thereby improving overall system performance.

Intellectual Property

- **IITM IDF Ref. 1467**
- **IN 487682 (Patent Granted)**

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Key Features / Value Proposition

- **Gain and offset calibration**, **error-compensating circuit architecture, phase error measurement** without a reference, integrated circuit chip implementation.
- **Improved performance** in **signal processing ICs, communication devices** with **reduced phase errors, enhanced accuracy, and simplified integration**.

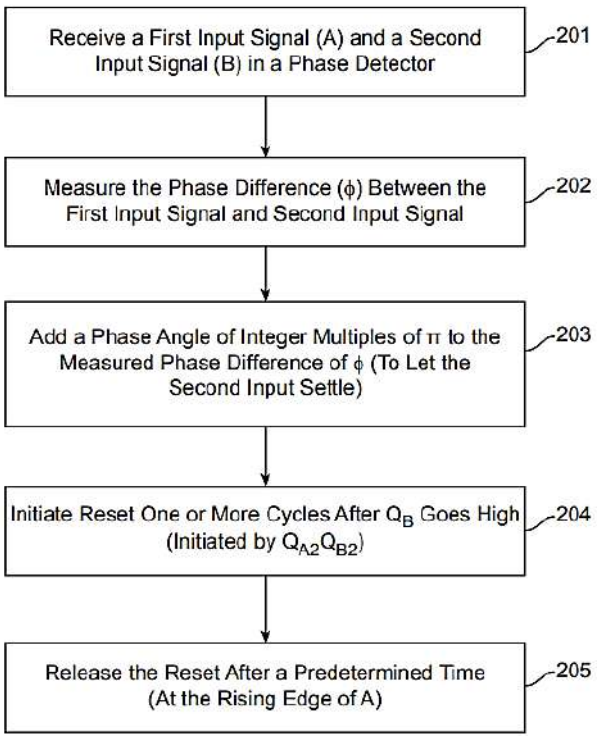

FIG. 2: illustrates the flowchart of the method of error compensation in a circuit receiving signals

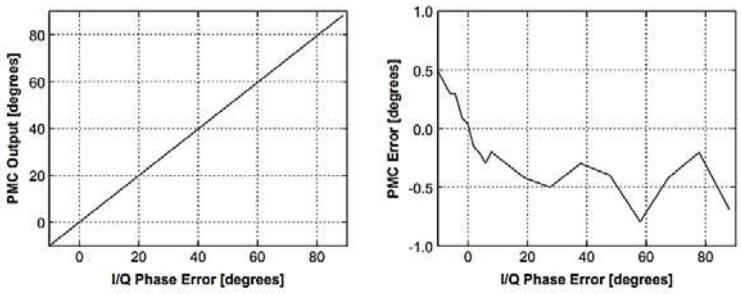

FIG. 3 illustrates the simulated characteristics of the proposed PMC.

Image

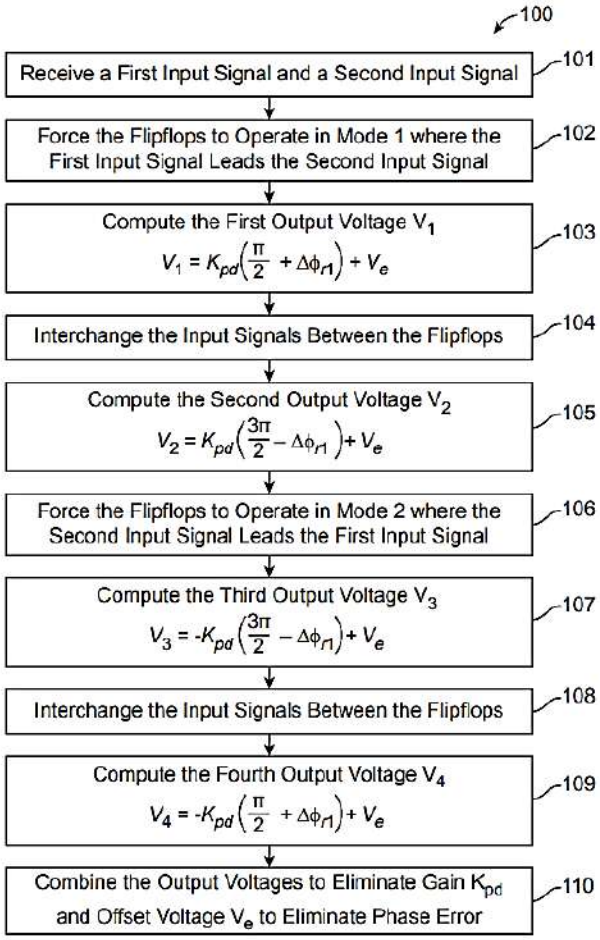

FIG. 4 illustrates the flowchart of the method of eliminating the phase error in a circuit receiving two or more input signals.

TRL (Technology Readiness Level)

TRL- 4, Technology Validated in lab

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