IIT MADRAS
Indian Institute of Technology Madras

Technology Transfer Office
TTO – IPM Cell

Industrial Consultancy & Sponsored Research (IC&SR)

SYSTEM AND METHOD FOR A CONTINUOUS TIME PIPELINED ANALOG-TO-DIGITAL CONVERTER WITH IMPLICIT DECIMATION

IITM Technology Available for Licensing

Problem Statement

- A pipelined analog-to-digital converter (ADC) is one of the most popular ADC architectures for sampling rates from a few mega samples per second (Msps) up to several Giga samples per second (GS/s).
- Despite their popularity in speed, resolution, dynamic performance, and low power consumption, face issues such as dependency on aliasing errors, driver amplifiers, Inadequate Error Removal etc.

Technology Category/ Market

Category – Computer Hardware, Software & Algorithm
Applications -CCD imaging, cable modems, and digital receivers, base stations, fast Ethernet, ultrasonic medical imaging, dsl technologies, digital videos
Industry – IT-Hardware
Market -The IT Hardware Market size is estimated at USD 130.86 billion in 2024, and is expected to reach USD 191.03 billion by 2029, growing at a CAGR of

Key Features / Value Proposition

❖ ***Technical Perspective***

- The power dissipation of the CTP ADC is claimed to be reduced by implicit **decimation achieved by operating the filter and the back-end ADC at the lower rate** than the predefined sampling frequency, while at least one pipelined stage operates at the predefined sampling frequency.
- The back-end ADC is specified to include at least one of a **Successive Approximation (SAR) ADC or any other type of ADC.**

❖ ***User Perspective***

- The CTP -ADC can operate at a fraction of regular computation frequency, thus providing significant computational power savings
- CTP -ADC with implicit decimation, with a simplified design that requires **lesser components.**
- Usage of the decimation factor enables simplified front-end stages and realization of a higher resolution back-end ADC which is **power-efficient.**
- CTP-ADC can enable larger DC gain of each stage, thus reducing resolution of the back-end ADC.

Technology

Includes a system for a Continuous Time Pipelined (CTP) Analog-to-Digital Converter (ADC) with implicit decimation comprising the following:

Pipelined Stage:
At least one pipelined stage configured to operate at a predefined sampling frequency

Filter: *configured to operate by decimating the predefined sampling frequency to a lower rate using a specified decimation factor*

Back-End ADC:
configured to digitize a filtered and amplified residue signal from the filter

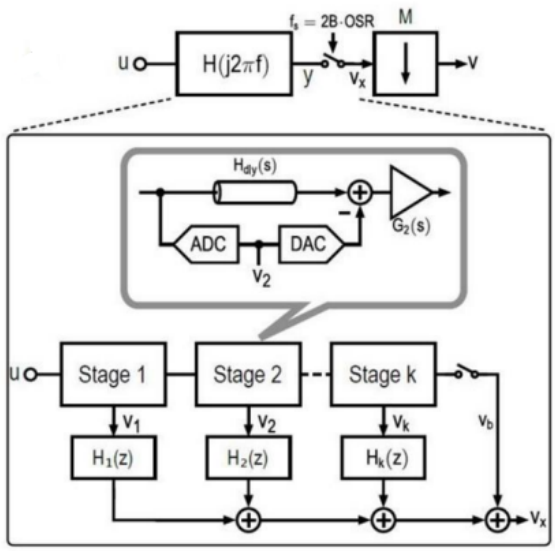

Fig. 1 depicts/illustrates an analog-to-digital converter (ADC) with implicit decimation, comprising a filter whose output is sampled and decimated by a factor M

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Images

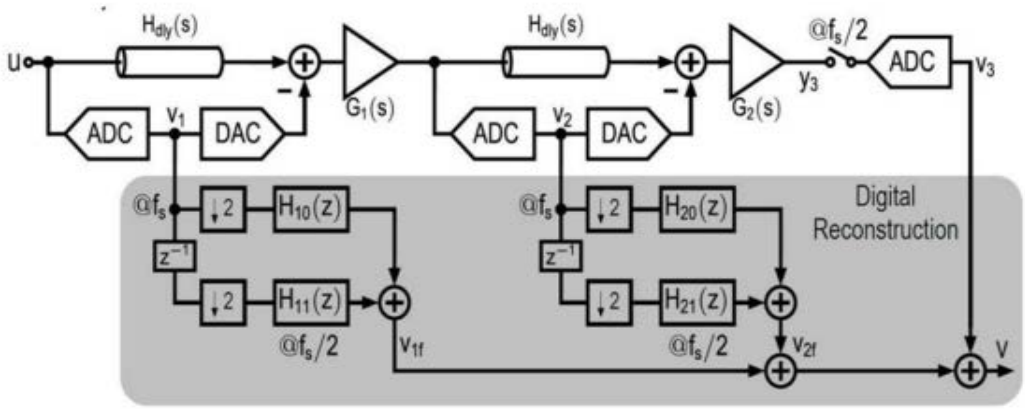

Fig. 2 depicts/illustrates an exemplary two-stage Continuous Time Pipeline ADC with implicit decimation, where pipelined stages operate at fs, back-end ADC operates at 0.5*fs, and digital reconstruction filters operate at half rate

Further discloses a method for a continuous time pipelined (CTP) analog-to-digital converter (ADC) with implicit decimation includes:

determining a number of pipelined stages, a number of filters, a decimation factor of the CTP ADC to operate at a predefined sampling rate by using a computing unit

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decimating the predefined sampling rate of at least one filter from the number of filters to a lower rate of the predefined sampling rate by using the determined decimation factor

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decimating the predefined sampling rate of a back-end ADC to the lower rate by using the determined decimation factor

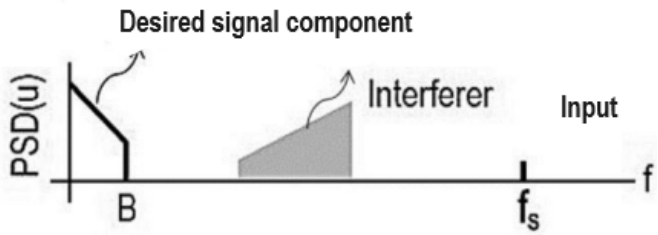

Fig.3 depicts/illustrates a graphical representation of an input spectrum comprising a desired signal component and an undesired out-of-band interferer signal

Intellectual Property

- **IITM IDF Ref. 2302**
- **IN454121-Granted**

Research Lab

Prof. SHANTHI PAVAN
Dept. of Electrical Engineering

TRL (Technology Readiness Level)

TRL-4,Technology Validated in the Lab

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