# PSEUDO-INTERDIGITATED-CORBINO THIN FILM TRANSISTOR WITH MULTI-FINGER SOURCE AND DRAIN ELECTRICAL CONTACTS

## IITM Technology Available for Licensing

### Problem Statement

- **Thin film transistors (TFTs)** are being widely used for various electronic applications. Achieving the three desirable properties of- **high transconductance**, **infinite output resistance**, and **reduced parasitic leakage** in a limited layout space helps in adapting TFTs for logic-TFT or driver-TFT applications.
- TFTs **with interdigitated electrodes and Corbino geometry** may enable increase in transconductance and reduction in parasitic leakage current with infinite output resistance respectively.
- However, **conventional technologies** despite using low-cost polymeric semiconductors and Corbino geometry are able to **achieve only infinite output resistance** while **not addressing the desired properties of high transconductance and reduction in parasitic leakage**.
- There is a need for a **simple fabrication** approach to **simultaneously achieve** excellent electrical isolation, increased transconductance and infinite output resistance while **accommodating a large channel width.**

### Intellectual Property

- IITM IDF Ref.**2789**
- Patent Application No: **IN 202441025688**

### TRL (Technology Readiness Level)

**TRL 4 Technology Validated in Lab**

### Technology Category/ Market

**Category- Electronics & Circuits**
**Industry Classification:**

- **NIC (2008)-2610-** Manufacture of electronic components
- **NAICS (2022)- 334413-** Semiconductor and Related Device Manufacturing**; 333242-** Semiconductor Machinery Manufacturing

**Applications:** Manufacture of Semiconductors, Thin Film Transistors (TFTs), micro-fluidic devices, electrodes, LED displays, RF-ID tags, flexible electronics and communication devices such as antennas, frequency selective surfaces etc.

**Market drivers:**
Global Thin Film Transistor market was valued at USD 180.9 Million in 2023 and is expected to grow to USD 821.5 Million by the end of 2030 with a CAGR of 24.2%

### Research Lab

**Prof. Soumya Dutta**
Dept. of Electrical Engineering, IITM

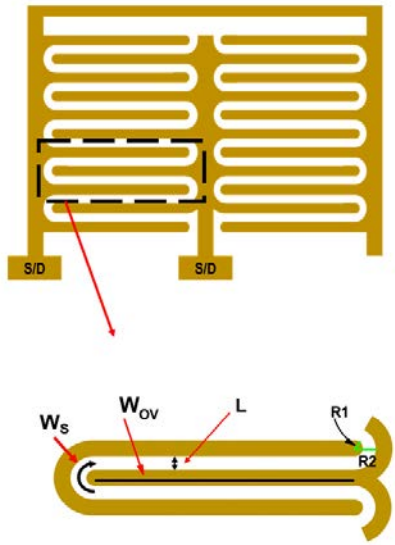


**Figure:** The novel Pseudo-interdigitated-corbino TFT architecture with optimized design having channel length L and the inner and outer radius R1 and R2, respectively, of half of the corbino disks with average channel width $W_S$; and overlapping linear channel regions with channel width $W_{OV}$

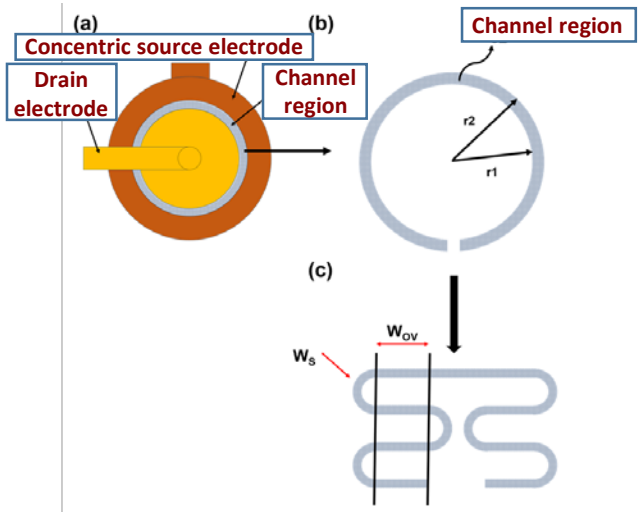


**Figure: (a)** Represents a top schematic of a concentional circular Corbino TFT **(b)** having the circular channel region with inner and outer radius r1 and r2, modified into a partially shielded Corbino structure **(c)** and further enveloped into an arrangement of overlapping linear channel regions with channel width $W_{OV}$ and half of the corbino disks with average channel width $W_S$

**CONTACT US**
**Dr. Dara Ajay, Head TTO**
Technology Transfer Office,
IPM Cell- IC&SR, IIT Madras

**IITM TTO Website**:
https://ipm.icsr.in/ipm/

**Email**: headtto-icsr@icsrpis.iitm.ac.in
tto-mktg@icsrpis.iitm.ac.in
**Phone**: +91-44-2257 9756/ 9719

# IIT MADRAS
Indian Institute of Technology Madras

## Technology Transfer Office
## TTO – IPM Cell

## Industrial Consultancy & Sponsored Research (IC&SR)

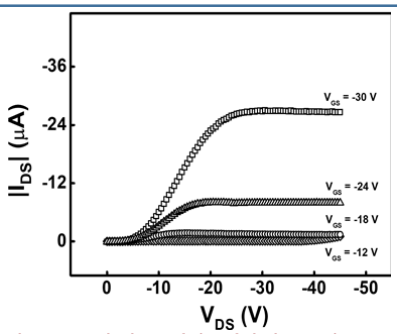


**Figure:** Output characteristics of the fabricated DPP-DTT semiconductor-based TFT arranged in the novel Pseudo interdigitated-corbino architecture shows flat output characteristics beyond-pinch-off displaying the infinite output resistance character in the saturation region.

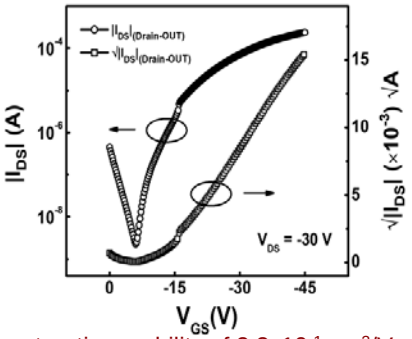


**Figure:** The saturation mobility of $2.3 \times 10^{-1}$ $cm^2/V\text{-}s$ and the on/off ratio of $10^5$ has been calculated from the saturation transfer characteristics of the device shown in The device showed a threshold voltage of -10 V.

## Technology

**The novel Psuedo-interdigitated-corbino TFT architecture comprises an arrangement of the source and drain electrodes to accommodate the large channel width (W) of the TFT in an enclosed interdigitated pattern. It is achieved by realizing an equivalent pseudo-corbino structure design as a combination of half-corbino structure and overlapping linear channels.**

**TFT using the novel Pseudo-interdigitated-corbino architecture results in infinite output resistance, providing constant drain output current in the saturation region independent of drain bias**

**The width of the overlapping linear channel region, denoted as $W_{OV}$ should be equal to or greater than two times the $W_S$ For a pseudo-interdigitated-corbino architecture with "n" number of interdigitated overlapping linear channels, the total channel width $W_t$ is given by $\{n.W_{OV} + (n-2).W_S\}$, where "n" is the number of interdigitated overlapping linear channels.**

**The average width of half of the corbino disk (WS) is calculated using the middle circumference approximation $\{\pi(R1+R2)/2\}$ as a function of geometrical parameters R1 and R2 i.e., the inner and the outer radius of half of the corbino disk with average channel width WS**

**The semiconductor layer is formed over or below the said source and drain electrodes in the top-gate top-contact, top-gate bottom-contact, bottom-gate bottom-contact, or bottom-gatetop-contact configuration.**

## Key Features / Value Proposition

- The architecture comprises a more readily manufacturable TFT architecture that offers infinite output resistance to provide constant drain current in the saturation region.
- The device showed excellent performance in terms of the device parameters. Whereas, none of the conventional methods overcome the limitations of multi-finger and Corbino TFT architectures in attaining excellent electrical isolation, increased transconductance and infinite output resistance, simultaneously, while accommodating high W/L ratio
- The novel Pseudo-interdigitated-corbino architecture results in an easily manufacturable TFT architecture with reduced fabrication process steps compared to conventional Corbino TFT architecture.

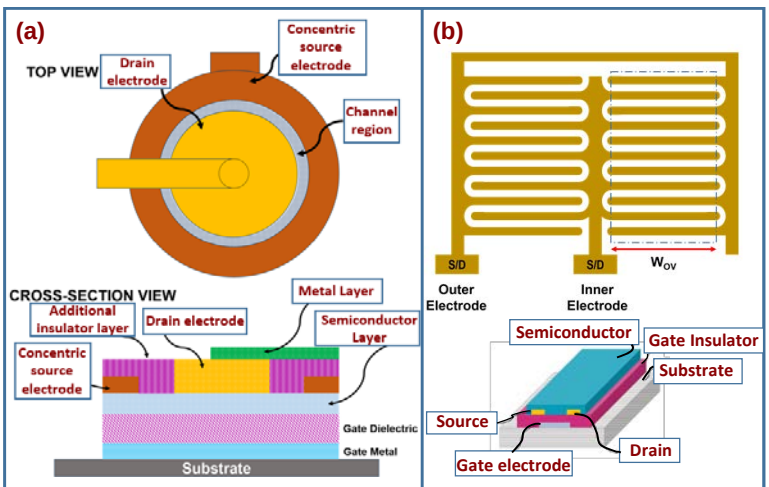


**Figure:** The main drawback of **(a)** conventional circular corbino is the increase in the number of added mask steps, resulting in no net mask count savings; Whereas in **(b)** the invented architecture with a compromised corbino geometry, called pseudo-corbino geometry, has an outer electrode element that partially shields the central electrode element requiring no additional patterning to access the central electrode element.


**CONTACT US**

**Dr. Dara Ajay, Head TTO**
Technology Transfer Office,
IPM Cell- IC&SR, IIT Madras

**IITM TTO Website**:
https://ipm.icsr.in/ipm/

**Email**: headtto-icsr@icsrpis.iitm.ac.in
tto-mktg@icsrpis.iitm.ac.in

**Phone**: +91-44-2257 9756/ 9719