A SIGNAL STRENGTH INDICATOR CIRCUIT

IITM Technology Available for Licensing

Problem Statement

- The problem statement discussed in the present invention is ***how to develop a topology where amplification and amplitude detection can be combined in a single block. .***
- Hence, subject invention addresses the issue efficiently.

Technology Category/ Market

Technology: Signal Strength Indicator Circuit;
Industry/Application: Signal Strength detectors, signal-strength detector; CMOS inverter;
Market: The global market is projected to reach at a **CAGR** of **32.58%** during the period **(2024-32).**

Technology

- Present patent discussed about a **pseudo-differential amplifier chain.**
- Said pseudo-differential amplifier chain comprises a **complementary metal oxide semiconductor (CMOS)** inverter pair as amplifier, configured to receive a differential signal.
- Further, it includes a **voltage regulator unit** connected to the pseudo-differential amplifier chain to provide a supply voltage Vs for biasing the pseudo-differential amplifier at a reference Direct current (DC) operating point.
- Moreover, the pseudo-differential amplifier chain includes a **current mirror circuit** connected with the pseudo-differential amplifier chain to receive a supply current from the pseudo-differential amplifier chain & generate a **mirrored output current**.
- The mirrored output current is used to determine **strength of the differential signal.**

Research Lab

Prof. Nagendra Krishnapura;
Dept. of Electrical Engineering

TRL (Technology Readiness Level)

TRL-4, Technology validated in Lab;

Intellectual Property

IITM IDF Ref. 2529; Patent No. 545473;

Images

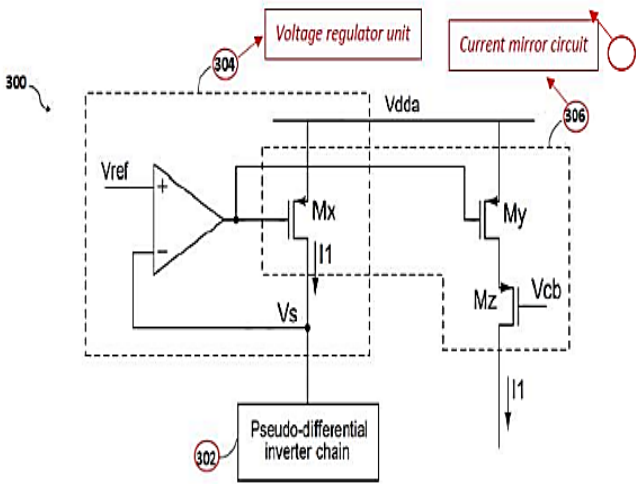

Fig.1 shows a block diagram for a signal strength indicator,

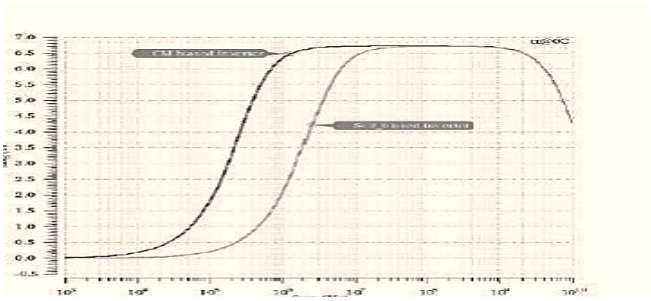

Fig.2 illustrates a frequency response of input to the output of pseud-differential inverter stage in self-biasing and common mode biasing of inverters,

CONTACT US
Dr. Dara Ajay, Head TTO
Technology Transfer Office,
IPM Cell- IC&SR, IIT Madras

IITM TTO Website:
https://ipm.icsr.in/ipm/

Email: headtto-icsr@icsrpis.iitm.ac.in
tto-mktg@icsrpis.iitm.ac.in
Phone: +91-44-2257 9756/ 9719

Industrial Consultancy & Sponsored Research (IC&SR)

Key Features / Value Proposition

- Integrates amplification & amplitude detection in a single unit. CMOS inverters can be more easily designed at low supply voltages than other types of amplifiers.
- Facilitates a compact signal-strength detector.
- Develops a signal-strength detector utilising low power.
- More amenable to low supply voltage operation.
- The signal-strength detector circuit occupies 0.08 mm², consumes 1.2 mW from 1.5V and
- the noise floor is 0.2mV rms. (Refer Table1)
- A 65nm prototype of the
- signal-strength detector circuit has a 70.9dB dynamic range with ±1dB error.

Images

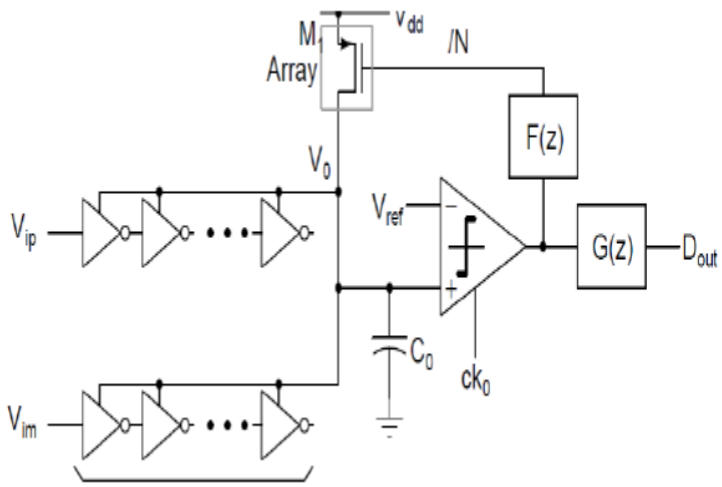

Fig.2 depicts a signal strength indicating circuit using a pseudo-differential inverter amplifier with a digital loop;

Process	65 nm CMOS	
Area	mm^2	0.08
Supply voltage	V	1.5
Power dissipation	mW	0.54
Dynamic range	dB	70
Log conformance error	dB	± 1
Noise floor	dBVp pd	−65
Bandwidth	MHz	1-22
Number of stages		6
Stage gain	dB	15.6

Table 1 shows performance summary of the signal strength detecting circuit ;

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IPM Cell- IC&SR, IIT Madras

IITM TTO Website:
https://ipm.icsr.in/ipm/

Email: smipm-icsr@icsrpis.iitm.ac.in
sm-marketing@imail.iitm.ac.in
Phone: +91-44-2257 9756/ 9719