IIT MADRAS
Indian Institute of Technology Madras

Technology Transfer Office
TTO – IPM Cell

Industrial Consultancy & Sponsored Research (IC&SR)

A hybrid analog to digital converter and method thereof

IITM Technology Available for Licensing

PROBLEM STATEMENT

- **ADCs enable digitally controlled circuits** to communicate with the real world.
- Analog signals have continuously **varying values from various sources and sensors.**
- Digital circuits work with binary numbers with two discrete states.
- An **ADC takes a snapshot of an analog quantity** at one instant and produces a digital output code.
- The **number of binary digits used to represent this analog voltage** value depends on the resolution of an A/D converter.
- **SSADC, a type of ADC, employs subtraction** technique to result in different bit status in different stages of conversion.
- SSADC has disadvantages such as **reduced bandwidth and noise level, making** it only implemented for 8-bit or 10-bit resolution.
- There is a **need for an analog to digital converter that can be implemented for bits higher than 8-bit or 10-bit resolution**.

TECHNOLOGY CATEGORY/ MARKET

Technology: A hybrid analog to digital converter and method
Category: Electronics & Circuits
Industry: Electronic System & Design Manufacturing (ESDM), Robotics
Application: Analog to Digital converter
Market: The global market size is expected to grow at a **CAGR of 6.3% during 2022-2030**, to surpass **US$ 6.29 Billion by 2030.**

INTELLECTUAL PROPERTY

IITM IDF Ref. 2313
Patent No: IN 551010

TRL (Technology Readiness Level)

TRL-4, Experimentally validated in Lab;

Research Lab

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TECHNOLOGY

1. •**Analog to Digital Converter**
2. •**First stage: Comprises first type cascaded blocks,**each with a comparator and subtractor.
3. •**Comparator**: Receives input signal and generates digital value when it's greater than or equal to a corresponding voltage divider value
4. •**Subtractor:** Determines a subtracted voltage value from the input signal and provides it as input to a subsequent cascaded block of the first stage.
5. •**Second stage:** Comprises **second type cascaded blocks,**each containing first type cascaded blocks .
6. •Each first type **cascaded block is interlinked to an amplifier** , amplifying converted bits.
7. •Second stage **conversion results in high resolution bits** due to amplified converted bits.
8. •**Amplifier:** Amplifies the predefined number of **converted bits of each first stage to provide an output to a subsequent second-type cascaded block,** enabling higher bit resolution.

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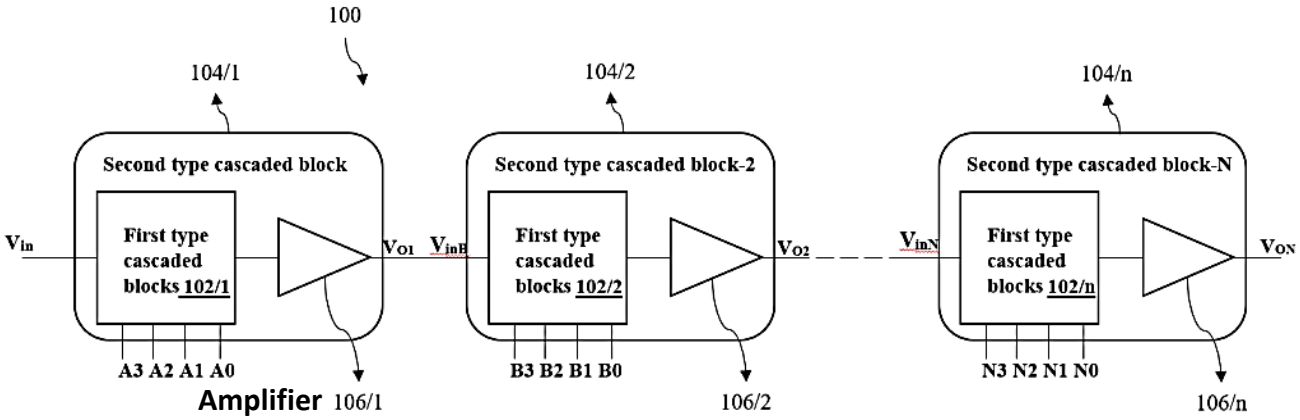
Fig. 1 illustrates a schematic diagram of a hybrid SSADC (Successive Subtraction Analog to Digital Converter)



Key Features / Value Proposition

Hybrid ADC Structure and Implementation

- The hybrid ADC includes a Hybrid Successive Subtraction Analog to Digital Converter (HSSADC) with stages and reference types.

Stages and Resolution:

- The first and second stage blocks may feature an N-reference 5 SSADC, with resolutions of 12-bit, 16-bit, or 20-bit.

Cascading Blocks:

- The architecture allows for cascading a predefined number of first-type and second-type blocks.

Voltage Divider Implementation:

- The corresponding voltage divider values for each cascaded block are based on voltage levels within a voltage divider network.

Digital Output Mechanism:

- The digital value from the comparator indicates a change in the state of the corresponding bit in the first-type cascaded block when the input signal meets or exceeds the voltage divider value.

Bit State Change:

- The method specifies changing the bit state to at least one of 1 or 0 within the predefined number of bits.

Incorporating N-reference SSADC:

- An N-reference Successive Subtraction Analog to Digital Converter (SSADC) is used in at least one of the first or second stage blocks.

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